Self-organized Germanium Quantum Dots/Si-based barriers for Semiconductor Charge Qubits

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Abstract — Advanced, robust CMOS technology is highly envisaged to facilitate the practical implementation of Si or Ge quantum dots (QDs) qubits and their charge-sensing devices for scalable quantum computing. The "holy grail" for QD device manufacturing is to achieve scalability through precise control and repeatable fabrication of Si-based QDs with desired shapes, sizes, and accurate placement for predictable electrical and optical properties. However, off-the-shelf nanometer-scale transistor processes cannot be directly transferred to physically-defined Si- and/or Ge-QDs qubit structures due to different operation principles. We will discuss the first-of-its-kind, CMOS technology for the implementation of germanium (Ge) QDs devices, including QD qubits for quantum registers and QD single-electron transistors for charge sensing. The technical challenges for the fabrication and operation of QD devices will be addressed from engineering perspectives. Based on our self-assembled Ge QD/Si-based (SiO_2, Si_3N_4, and Si) confinement barrier system using CMOS approaches, the controllable tunability on the QD diameter, barrier width/ height, and placement at the designated spatial-location in combination with self-aligned electrodes facilitate the implementation of a charge-qubit prototype using a double-QDs (DQDs) configuration. In this work, we presented a device and technology co-design of self-organized Ge QD/Si-based barriers system and demonstrated the functionality of a Ge-DQDs qubit and Ge-QD single-hole transistors (SHTs) via the steady-state transport diagrams measured at $T > 10$ K.